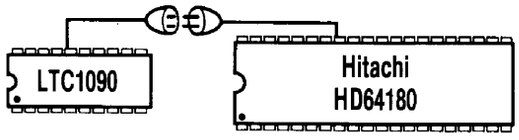
Interfacing the LTC1090 to the HD64180



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Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Hitachi 64180 microprocessor. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 64180 in 96μs. Configuration of the LTC1090 and the 64180 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a synchronous full duplex format over D_{IN} and D_{OUT}.

The 64180 has a clocked serial I/O port (CSIO) that allows the user to construct a simple communication path to the LTC1090. The serial port provides clock, transmit and receive lines that are compatible with the LTC1090. The only additional line required is one programmable output pin (RTSO) to control $\overline{CS}$ on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1090 was 2MHz and the 64180 crystal frequency was 4MHz. This produced a transfer time of 479μs. A version of the 64180 can be run at a 20MHz crystal frequency so the times shown can be reduced by a factor of five yielding a total transfer time of 96μs.

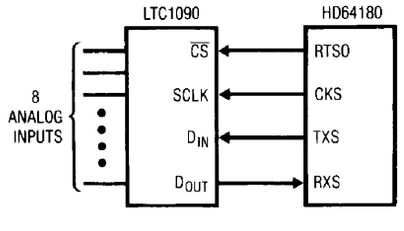

Figure 1. LTC1090 Transmits Data to HD64180 Using 4 Wires

At crystal frequencies up to 4MHz ACLK can be generated directly from the ϕ pin of the 64180. Above 4MHz a divider must be used to generate ACLK or it must be externally generated to ensure it remains below 2MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

Software Description

The software configures and controls the CSIO of the 64180. Additionally, the software manipulates RTSO ($\overline{CS}$ of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion. Because the CSIO of the 64180 communicates in a half duplex format it is necessary for the software to first write a configuration word to

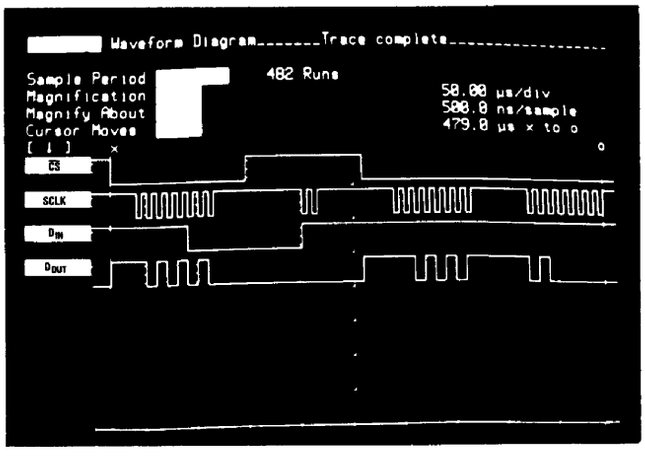

Figure 2. Timing Diagram. Transfer Times as Short as 96μs are Possible.

the LTC1090 and then read back the data. Normally with the LTC1090 the D_{IN} and D_{OUT} words are transferred simultaneously.

The software first disables all interrupts and enables the receive (RXS) pin. The D_{IN} word is loaded into the Transmit Receive Data Register. The D_{IN} word programs the LTC1090 for channel 7 with respect to common, LSB first, unipolar and eight bits as shown in Figure 3. Note, that for LSB first format processors the D_{IN} word must be constructed opposite from MSB first format. This is because the bits forming the D_{IN} word of the LTC1090 must always be shifted in the same order regardless of whether MSB first or LSB first is chosen. B4 of CNTLA0 is cleared which causes $\overline{CS}$ of the LTC1090 to go low. B4 of the CSIO control register is set which causes the D_{IN} word for the LTC1090 to begin transmitting. B7 of the CSIO control register is polled until a 1 is detected. B4 of CNTLA0 is then set which causes $\overline{CS}$ to go high.

Forty-four ACLK cycles must pass before $\overline{CS}$ can be taken low so that the A/D can perform a conversion. During this time a transmit is started and stopped so that the TXS line will stop high. The transmit is not allowed to finish to save time. It is desirable to have the TXS line high so that the proper word length will be clocked into the LTC1090 when D_{OUT} is read.

$\overline{CS}$ of the LTC1090 is again cleared. The CSIO control register is set up to receive this time. The transmit line is held high so that all ones are clocked into the LTC1090 D_{IN} pin while the LSBs of D_{OUT} are being clocked into the 64180. The same polling method is used as before. After the first eight bits are received the data is stored in Register L. The two MSBs are then clocked in and placed in Register H. The data at this point is right justified with the unused bits being set to 0s as shown in Figure 4. $\overline{CS}$ of the LTC1090 is then set again.

Because the D_{IN} word received by the LTC1090 was a dummy word, it is not necessary to wait 44 ACLK cycles again at this point. The $\overline{CS}$ line can be brought low immediately and another cycle begun at this time.

0	0	0	1	1	1	1	1	
WL0	WL1	MSBF	UNI	S2	S1	O/S	S/D	REG D

Figure 3. D_{IN} Word for LTC1090 Stored in Reverse Order in 64180 Internal Registers

								LSB	
LSB	7	6	5	4	3	2	1	0	REG L
							MSB		
MSB	0	0	0	0	0	0	9	8	REG H

Figure 4. D_{OUT} from LTC1090 Stored in 64180 Internal Registers

Summary

A four wire interface between the LTC1090 and the Hitachi 64180 with a combined data conversion and transfer time of 96μs was demonstrated. The interface used the CSIO port of the 64180. Because the CSIO port transfers data LSB first care must be taken in constructing the D_{IN} word so that the bits are transmitted in the proper order to the LTC1090. A configuration word is written to the LTC1090 in one eight bit transfer and then the 10 data bits of the LTC1090 are shifted LSB first to the 64180 in two eight bit transfers. The data is stored right justified in the 64180's internal registers.

ADDR	LABEL	CODE	MNEMONIC	COMMENTS
0	BEGIN	F3	DI	DISABLE INTERRUPTS
1		1E 00	LD E, 00H	DATA FOR ASCI STATUS REG
3		ED 19 05	OUT0 (05H), E	ENABLE RXS
6	LOOP	16 1F	LD D, 1FH	LOAD D_{IN} IN REG D
8		ED 11 0B	OUT0 (0BH), D	LOAD D_{IN} IN TRDR
B		1E 00	LD E, 00H	DATA FOR CNTLA0
D		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. $\overline{CS}$ RESET
10		1E 10	LD E, 10H	DATA FOR CSIO CONTROL REG
12		ED 19 0A	OUT0 (0AH), E	START TRANSMIT OF D_{IN}
15		0E 0A	LD C, 0AH	ADDR OF CSIO CONTROL REG
17	TX1	ED 74 80	TSTIO 80H	
1A		28 FB	JR Z TX1	WAIT FOR TRANSFER TO END
1C		1E 10	LD E, 10H	DATA FOR CNTLA0
1E		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. $\overline{CS}$ SET
21		16 FF	LD D, FFH	DUMMY DATA WORD
23		ED 11 0B	OUT0 (0BH), D	LOAD DUMMY IN TRDR
26		1E 10	LD E, 10H	DATA FOR CSIO CONTROL REG
28		ED 19 0A	OUT0 (0AH), E	START TRANSMIT OF DUMMY
2B		1E 00	LD E, 00H	DATA FOR CSIO CONTROL REG
2D		ED 19 0A	OUT0 (0AH), E	STOP TRANSMIT OF DUMMY
30		ED 20 0B	IN0 H, (0BH)	CLEAR EF OF CSIO CNTRL REG
33		1E 00	LD E, 00H	DATA FOR CNTLA0
35		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. $\overline{CS}$ RESET
38		1E 20	LD E, 20H	DATA FOR CSIO CNTRL REG
3A		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} LSBs
3D	RX1	ED 74 80	TSTIO 80H	
40		28 FB	JR Z RX1	WAIT FOR TRANSFER TO END
42		ED 28 0B	IN0 L, (0BH)	PUT LSBs IN REG L
45		ED 19 0A	OUT0 (0AH), E	RECEIVE D_{OUT} MSBs
48	RX2	ED 74 80	TSTIO 80H	
4B		28 FB	JR Z RX2	WAIT FOR TRANSFER TO END
4D		ED 20 0B	IN0 H, (0BH)	PUT MSBs IN REG H
50		1E 10	LD E, 10H	DATA FOR CNTLA0
52		ED 19 00	OUT0 (00H), E	DATA IN CNTLA0. $\overline{CS}$ SET
55		C3 06 00	JP LOOP	DO NEXT CONVERSION

Figure 5. HD64180 Code Transfers Data to and from the LTC1090